Electrical and layouts simulation of analytical microsystem-on-chip elements for high frequence and low temperature applications

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Abstract. **In this paper the results of layout design and circuit-topological computer simulation of some elements of analytical microsytem-on-chip with the "silicon-on-insulator" (SOI)-structures are presented. These elements were: an input cascade, a basic element of operational amplifier and a ring oscillator based on standard bulk CMOS technology and CMOS technology with the SOI-structures. Also the polysilicon-on-insulator resistive elements were studied in the wide temperature range. Such elements can be used as regular elements matrix for analog and digital signal processing in the integrated circuits and initial processing of analytical information microsystem-on-chip or as sensitive elements of the intellectual sensors of microsystem-on-chip.**

Keywords: analytical microsystem-on-chip, operational amplifier, matrix basic cell, SOI-structures, gate array, sensor element.

I. Introduction

The electronic devices for both normal and special conditions are used in the modern information systems. That is why the studies and development of microelectronic elements are important for such devices. Such microelectronic elements will provide work in conditions of high radiation, extended temperature range, high magnetic fields and perform signal processing with high speed [1-5]. In addition, to solve the problems necessary devices based on micro- and nanoelectronic technologies, and monolithic integration non silicon elements in the silicon crystal and to study their characteristics directly in the crystal.

One of such devices as a tool for analysis of new integrated elements, including non silicon technology or other physical objects with micro- or nanometer sizes directly in the crystal could be Analytical Microsystem-on-Chip (AMSoC).

Need AMSoC due to the fact that obtaining such information from micro- and nano objects, connected through external probes or wires may be caused distortion of the initial information because of their parasitic properties.

It is therefore advisable to carry out studies such elements directly in AMSoC. In AMSoC would be the primary connection information directly to the micro- and nanometer sizes integrated elements from its primary processing and transformation. This AMSoC will process signals from the objects of study and transmission of processed and amplified signal to an external measuring or computerized devices.

To implement AMSoC important is its architecture, which would have made it possible in a short time to create a series of functionally specialized AMSoC. One of the approaches to the design of such systems could be custom-known method of designing integrated circuits (ICs) based on the matrix of regularly repeating layout elements with different functionalities.

Constructive and technological base for creation AMSoC could be standard CMOS technology. However, analysis of existing CMOS technology shows more promising structures "silicon-on-insulator" (SOI). SOI structures are much better both in terms of electrical characteristics and resistance to external influences compared to structures on the bulk silicon. SOI structures also have significant advantages as a constructive material for new device elements, including new three-dimensional structures [6, 7]. That opens additional prospects for new integrated device structures and extend the functionally possibilities of AMSoC.

Studies and development of integrated elements with SOI structures are necessary to create AMSoC N, as well as data on mutual layout parameters of real elements on a chip to electrical, time, temperature and other characteristics [8, 9]. Just this article is aimed at alleviating these problems.

II. Protection elements modelling of AMSOC input cascades

As AMSoC is a complex system made on the basis of SOI CMOS technology, its input cascades is sensitive to excess voltage input signals and static electricity. In this connection, protection schemes have been developed, consisting polysilicon resistor and two SOI diodes. One of SOI diodes limits the negative voltage, and other - positive voltage respectively in excess of the allowable threshold by connecting power to the supply or total bus. A development layout fragment of protection circuits, pad and SOI CMOS transistors matrix are shown in Fig. 1.

The time parameters simulation of signal propagation applied to the contact pad through protection scheme were carried out for both SOI CMOS structures and identical based on bulk CMOS structures. Simulations performed directly from the layouts taking into account the size of the parasitic elements and connections.

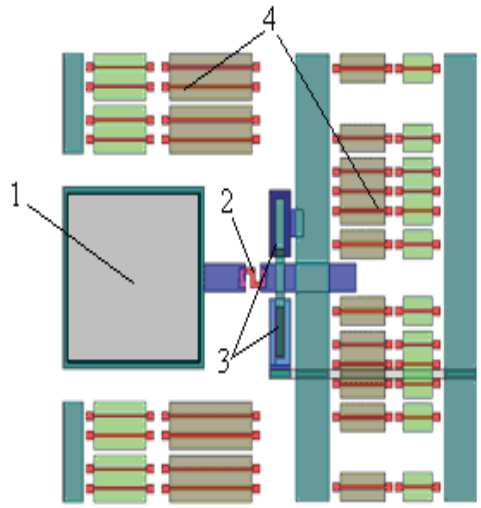


Fig. 1. Layout of protection circuits, pad and SOI CMOS transistors matrix: 1 pad; 2 – polysilicon resistor; 3 – protection SOI-diodes; 4 – SOI CMOS transistors matrix for input cascade

The input protection element is supplied sinusoidal signal at 1 GHz and amplitude of 10 V. Power supply AMSoC was 5 V. According to the simulation results established that the for protection elements based on bulk CMOS structures the signal delay of 7 ps, maximum current with 1.19 mA, power consumption of 8.88 mW. For protection element based on SOI structures the signal delay is 4 ps, the maximum current of 0.54 mA, power consumption of 6.89 mW. The simulation results of signals propagation via protection elements on SOI structures are shown in Fig. 2.

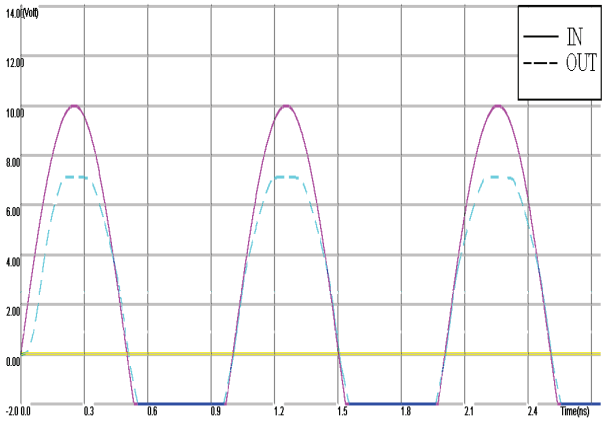


Fig. 2. The simulation results of signal propagation via protection elements on SOI structures

III. LAYOUT DESIGN AND SIMULATION OF SOI RING GENERATOR

To assess the frequency characteristics AMSoC elements based on CMOS SOI structures were designed and simulated a 7-cascade ring generator directly from the layouts. Ring generator can determine the performance of its structural elements, elements that can be manufactured at new technologies or scarcely explored. A ring generator layout modeling for seven inverters is shown in Fig. 3.

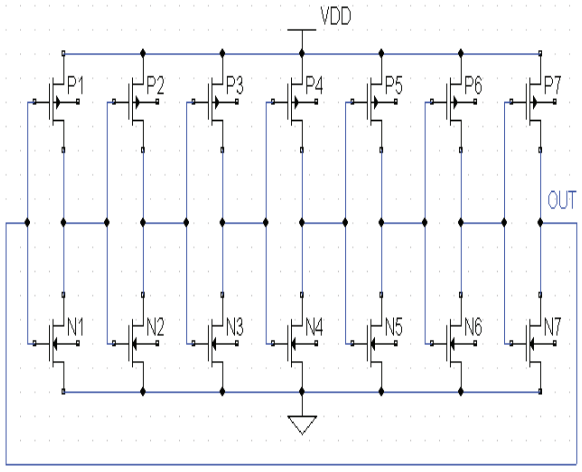


Fig. 3. The ring oscillator electrical circuit

This generator requires no external time depend schemes, its oscillation frequency depends on the number of inverters and time delay of everyone. AMSoC elements, including ring oscillator layouts (Fig. 4), developed on the matrix cells with SOI structure [9].

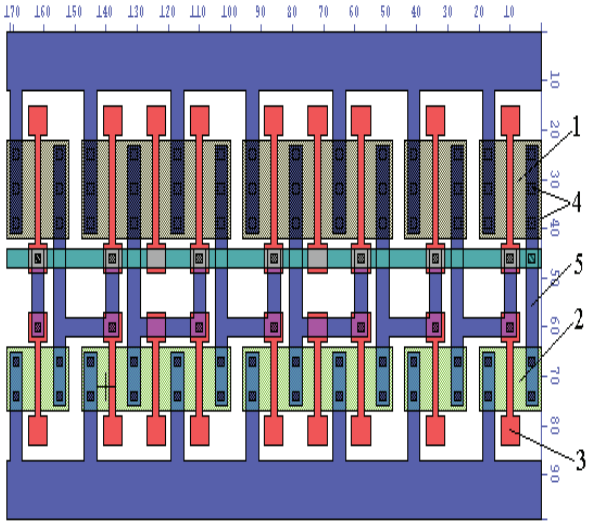
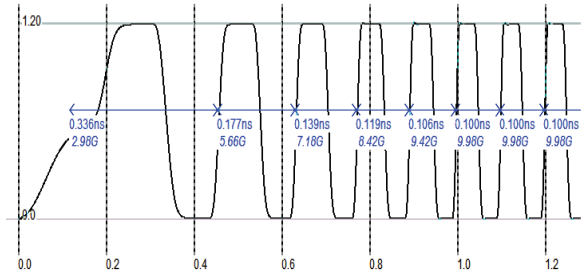
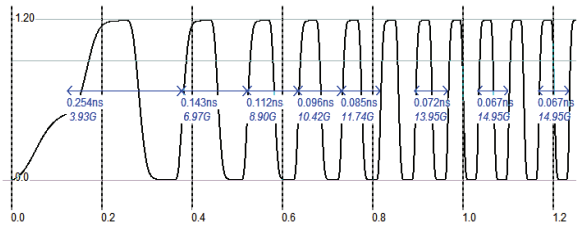


Fig. 4. The ring generator cell matrix based on the structure of SOI: 1 – source-drain p-channel MOS transistors; 2 – source-drain n-channel MOS transistors; 3 – polysilicon gates; 4 – contacts; 5 – metal connections

The simulation results of CMOS and SOI CMOS ring generators identical with the voltage of 1.2 V are shown in Fig. 5.



a)



b)

Fig. 5. Simulation results of the ring oscillator based on the matrix cells: a) bulk CMOS structure; b) SOI CMOS structure

By modeling the operating frequency of the studied CMOS ring generator was 9.98 GHz and power consumption of 189 μW. For SOI CMOS ring oscillator frequency was 14.95 GHz for the same supply voltage of 1.2 V.

Increasing of frequency at the same voltage for SOI CMOS ring generator is due to reduced parasitic capacitance in SOI CMOS elements. By reduce the voltage to 0.9V in the received frequency of 9.98 GHz CMOS generator similar to the supply voltage of 1.2V. Power consumption is decreased by 3 times compared to 68.4 μW with bulk CMOS structures.

IV. SOI CMOS OPERATIONAL AMPLIFIER BASIC ELEMENT

Important elements of processing and transformation the analog signals into AMSoC are integral operational amplifiers (OP), which are necessary to highlight and strengthen information signals that could be commensurate with a noise. These elements are the diagram comparing two signals and amplifying the difference of voltage. The coefficient of weakening phase signal is enough large. Electrical scheme of OP basic element in integrated performance is shown in Fig. 6.

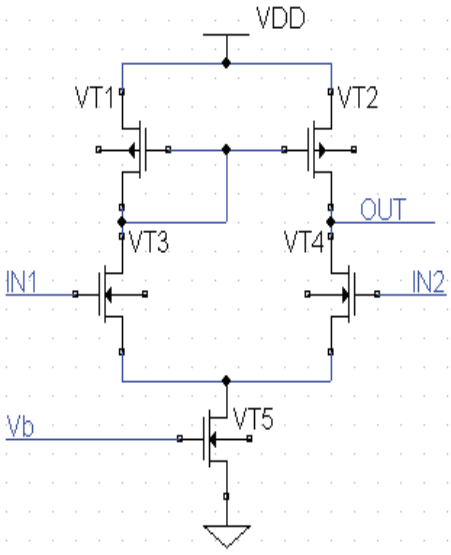
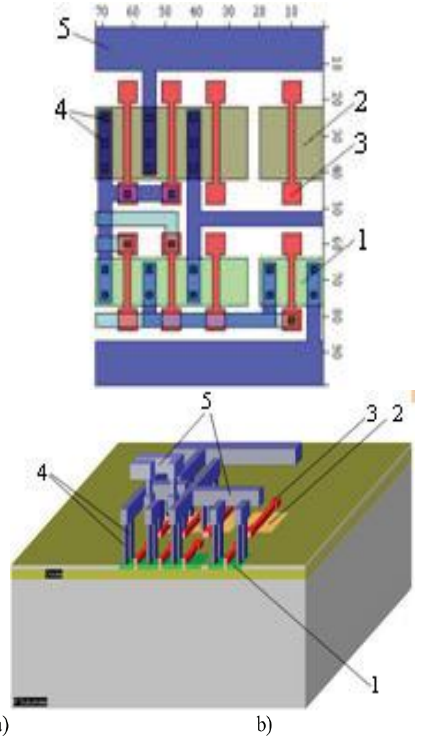


Fig. 6. The electrical circuit integrated operational amplifier: VT, VT2 – p-channel transistor of current mirrors; VT3, VT4 – n-channel transistors of differential pair; VT5 – transistor voltage control;. IN1, IN2 – common mode inputs; OUT – output

Designed layouts of OP basic element based on matrix cells consistent structural and technological parameters according to Fig. 6, is shown in Fig. 7. It was studied two OP layouts: with CMOS- and SOI CMOS technology.



a) b)

Fig. 7 .Layouts: a) and three-dimensional image; b) of integrated OP element based on the matrix cells with SOI-structure: 1 – source-drain- n - channel transistors; 2 – drain leakage field p- channel transistors; 3 – polysilicon gates; 4 – contacts; 5 – metallization

Comparative modeling results these elements directly from OP layouts are shown in Fig. 8.

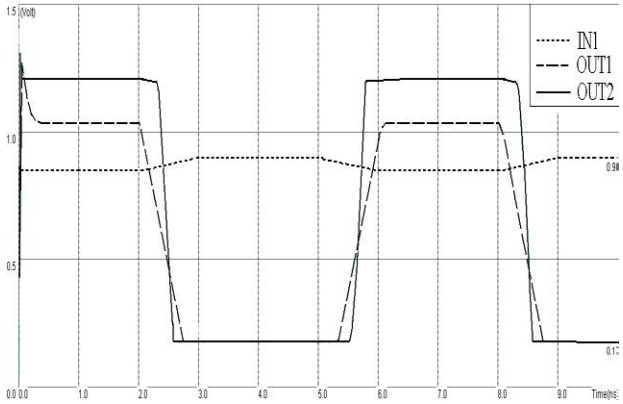


Fig. 8. Simulation results of OP: 1 – input signal IN1; OUT1 – output signal of CMOS OP; OUT2 – output signal SOI CMOS OP

In the simulation the power voltage was 1.5V, the input signal IN1 – sinusoidal signal with amplitude of 0.04 V, a frequency of 0.167 MHz, rise time and decay – 1 ns pulse duration – 2 ns. Input IN2 – constant amplitude of 0.7 V. The simulation results shown that the output signals for the circuit of SOI structures compared to bulk CMOS are significantly better on average 30% slope fronts and a larger gain, so the output signal amplitude level is 20% higher.

These parameters will significantly reduce power consumption during transients (impulses shorter duration fronts), and as a result, increase the degree of integration of elements in AMSoC. In addition, the implementation of OP based on SOI structures will expand the temperature range.

V. AMSOC RESISTIVE ELEMENTS ON BASE OF "POLYSILICON-ON-INSULATOR"

The test resistors structures as elements of AMSoC for electric properties measurement of polysilicon layers on insulator (Fig. 9) were designed. The dimensions of polysilicon resistor in polysilicon-on-insulator (PolyOI) structure were 80 μm × 8 μm × 0.5 μm. Two groups of samples have been studied with initial boron concentration of $2.4\times10^{18}cm^{-3}$. Improvement of technical performances of PolyOI-structure is achieved due to laser recrystallization of poly-Si. After the laser recrystalization the charge carriers concentration equals is $1.7\times10^{20}cm^{-3}$ by the Hall studies.

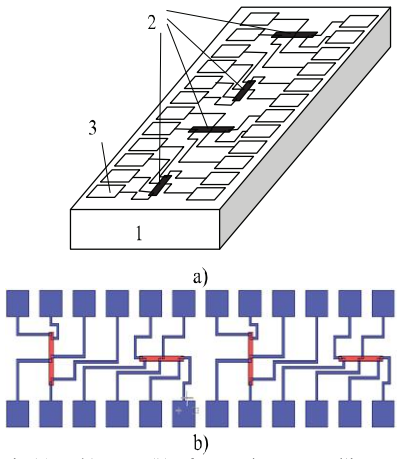


Fig. 9. Schematic (a) and layouts (b) of test resistors: 1 – silicon substrate, 2 – polysilicon resistors, 3 – contact pads.

The forming technology of test polysilicon resistors were described in [10, 11].

The impedance analysis method was used for testing the polysilicon resistors. This method is that the studied test resistor is excited by a small sinusoidal signal which is measured at the exit. These measurements were carried out in the frequency range 10^{-2}-10^{5} Hz by Lock-in Amplifier 7265 DSP (AMETEK). Diagram of experimental data [12, 13], or in other words Nyquist plot, serves as the dependence Z"(Z'), where Z" - imaginary resistance value and Z' - real resistance. On the basis of experimental frequency dependence Z" and Z' the building of equivalent electric circuits for analyzing the structure of the samples were carried out. The modulus of impedance was measured in frequency range from 0.01 Hz to 250 kHz in the temperature range 4,2-77 K.

Since the AC measurements are specific investigation methodology by which the samples characteristics were determined needs to be considered apart. The quadrupole theory was used to avoid the influence of measuring channels on experimental results obtained for AC measurements [14, 15].

VI. CONCLUSIONS

The need for research and development of AMSoC are substantiated. Comparative modeling of electrical and layout structural AMSoC elements, implemented on the matrix cells with SOI structures and structures on bulk silicon, for input cascades of the protection circuit, ring oscillator, an operational amplifier and polysilicon resistive elements.

It is shown that such elements of SOI structures have significant advantages over bulk silicon structures on the performance, temperature range and power consumption.

The results of the simulations show that these matrix elements on SOI structures are promising for creation new microelectronic devices.

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